Q1. Consider a digital computer has a memory unit of 64Kx16 and cache memory of 1K words. The cache uses direct mapping with 4 blocks size of four words.

1. How many bits are there in the tag, block, and word fields of the address format.
2. 6, 6, 2 b) 8, 6, 2 c) 2, 6, 8 d) 6, 8, 2

Ans: d)

Q2. In case of direct mapping of cache, the mapping is expressed as:

1. Cache line number = (main memory block number) modulo (number of lines in the cache)
2. Cache line number = (number of lines in the cache) modulo (main memory block number)
3. number of lines in the cache = (Cache line number) modulo (number of lines in the cache)
4. number of lines in the cache = (number of lines in the cache) modulo (Cache line number)

Ans: a)

Q3. If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10 ns memory) is \_\_\_\_\_\_\_\_\_\_

1. 93% b) 87% c) 88% d) 90%

Ans: d)

Q4. If the cache needs an access time of 20 ns and the main memory 120ns, then the average access time of a CPU is (assuming hit ration is 80%)

1. 40ns b) 35ns c) 30ns d) 45ns

Ans: a)

Q5. For a memory system, hit time is given as 2 ns with miss rate of 1.5% and miss penalty of 60 ns then average access time is

1. 2.98 ns b) 2.9 ns c) 4.19 ns d) 3.98 ns

Ans: b)

Q6. For a memory system, the average access time is 4.5 ns with hit time 3 ns and miss rate of 2.5% then miss penalty is

1. 80 ns b) 100 ns c) 60 ns d) 55 ns

Ans: c)

Q7. The memory read operation takes 20 ns as cache access time, and 28 ns as main memory access time, h = 6/7 then what will be the mean access time

1. 16ns b) 48ns c) 28ns d) 24ns

Ans: d)

Q8. For a machine assume that the cache miss penalty is 50 clock cycles, and all instruction normally takes 2 clock cycles. Assume that the miss rate is 2% and there is an average of 1.33 memory references per instruction. What is impact on performance when behaviour of cache is included?

1. 68.5 b) 58.7 c) 78.2 d) None of these

Ans: a)

Q9. A block set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight-bit word.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET, and WORD fields.
3. 22; 9, 5, 8 b) 22; 5, 8, 9 c) 24; 9, 5, 8 d) 24; 5, 8, 9

Ans: a)

Q10. Consider a cache memory (M1) and memory (M2) hierarchy with following characteristics:

M1: 16K word, 50ns Access time

M2: 1M word, 400ns Access time

Assume 8-word cache blocks and set size 256 words with set associative mapping. Calculate the effective memory access time with cache hit ratio= 0.95

1. 50ns b) 30ns c) 70ns d) 90ns

Ans: c)

Q11 Q1 Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find-

1. Number of bits in tag
2. Tag directory size

Q2. Consider a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find-

1. Size of main memory
2. Tag directory size

Q3. Consider a direct mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find-

1. Size of cache memory
2. Tag directory size

3. No. of physical address bits

4. No. of bits in block offset